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EXAMINER	
SHEW, JOHN	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,729	CHEN ET AL.	
	Examiner	Art Unit	
	John L. Shew	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,7,8,11-32,35,37,38 and 41-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30,41-45* is/are rejected.

7)☒ Claim(s) *1,2,5,7,8,31,32,35,37,38 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/7/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1, 31 are objected to because of the following informalities:

Claim 1, line 6 cites "said plurality" should be "a plurality".

Claim 1, lines 12-13 cites "said release count value" should be "a release count value".

Claim 31, line 8 cites "said plurality" should be "a plurality".

Claim 31, lines 14-15 cites "said release count value" should be "a release count value".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-14, 16-28, 30, 41-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basso et al. (Pub. No. US 2002/0154634 A1), Tezuka (Patent No. US 6658014 B1), Gulick (Patent No. 4809269), and further in view of Hooper (Pub. No. US 2003/0043803 A1).

Claim 11, Basso teaches an apparatus comprising an input module to store packet data within a storage element (Fig. 2, the reception of data packets from the input Ethernet

MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic ref. by page 3 para. [0059], page 4 para. [0060], [0069]), and to initialize a transmit count value of said storage element (MCC of Fig. 5, MultiCast Counter value stored by the Dataflow Chip based on the multicast action ref. by page 5 para. [0084]-[0085], page 6 para. [0104]-[0106]), a direct memory access controller to transmit said packet data from said storage element (Fig. 2, Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), and to de-allocate said storage element in response to a determination that said transmit count value is equal to a release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the comparison of the MCC to the value of zero followed by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues.

Basso does not teach a processing element to determine a release count value of said storage element nor a memory controller incrementing said transmit count value by one in response to transmitting said packet data nor storage of count values within said storage element.

Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, col. 16 lines 17-31, Release Count Designation Unit 22-4 of Fig. 23, Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output ref. by col. 18 lines 60-67, col. 19 lines 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Basso and Tezuka do not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data nor storage of count values within said storage element.

Gulick teaches a memory controller incrementing said transmit count value by one in response to transmitting said packet data (Transmit Byte Counter 154 of Fig. 5, Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached ref. by col. 10 lines 29-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Basso, Tezuka and Gulick do not teach storage of count values within said storage element.

Hooper teaches storage of count values within a storage element (transmit count stored in the primary packet descriptor ref. by page 3 para. [0025]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multicast data transmission method of Hooper to the dual port Packet Buffer Multicast Data Structure of Basso, Tezuka and Gulick for the purpose of using multiple transmit processors to transmit packets as suggested by Hooper (Abstract lines 1-6).

Claim 12, Basso teaches wherein said input module to store packet data within a storage element (Fig. 2, the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic ref. by page 3 para. [0059], page 4 para. [0060], [0069]), and to initialize a transmit count value of said storage element (Fig. 5, MultiCast Counter value stored by the Dataflow Chip based on the multicast action ref. by page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]), comprises an input module to receive a packet (Fig. 2, the Ethernet MAC interface 203 ref. by page 3 para. [0059]), including said packet data (message Data of Fig. 4), and to allocate said storage element for said packet including said packet data (Fig. 2, the Dataflow chip 202 interfacing to a large Datastore Memory 205 for buffering of traffic ref. by page 3 para. [0059], page 4 para. [0060], [0069]).

Claim 13, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of output

interfaces (Fig. 2, the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports ref. by Fig. 5, page 5 para. [0084]-[0086]).

Claim 14, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), via a plurality of output interfaces (Fig. 2, Fig. 5, the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports ref. by page 5 para. [0084]-[0086]), comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of line interfaces (Fig. 2, the Ethernet MAC interface 203 of various transmission protocol rates ref. by page 3 para. [0059]).

Claim 16, Basso teaches said packet data including a packet header (Fig. 4, the Message ID and Message Parameters ref. by page 5 para. [0075]-[0083]), and a packet body (Fig. 4, the Data ref. by page 5 para. [0075]-[0083]), wherein said input module to store packet data within a storage element (Fig. 2, the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic ref. by page 3 para. [0059], page 4 para. [0060], [0069]), and to initialize a transmit count value of said storage element (MCC of Fig. 5, MultiCast Counter value stored by the Dataflow Chip based on the multicast action ref. by page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]),

comprises an input module to store said packet body within a common storage element (Fig. 5, Buffers $505_1 - 505_5$ to store packet data ref. by page 5 para. [0084]-[0085]), comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports ref. by page 6 para. [0090]), and to associate each of said plurality of unique storage elements with said common storage element (the linkage of the FACB 503 to the Buffers $505_1 - 505_5$ of Fig. 5) . Basso does not teach said processing element to determine a release count value of said storage element. Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, the Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output ref. by col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Claim 17, Basso teaches an apparatus comprising a first line card to transmit data to a communications network (Fig. 2, the Ethernet MAC interface 203 ref. by page 3 para. [0059]), a line card interconnect coupled to said first line card and a second line card

coupled to said line card interconnect (Fig. 2, the interconnection between the Ethernet MAC interface 203 and the Dataflow Chip 202 ref. by page 3 para. [0059]), to receive data from a communications network (Fig. 2, the Dataflow Chip 202 transmitting and receiving traffic via network port ref. by page 3 para. [0059], page 4 para. [0060]), said second line card including an input module to store packet data within a storage element (FIG. 2, the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers ref. by page 3 para. [0059], page 4 para. [0060]), and to initialize a transmit count value of said storage element (MCC of Fig. 5, the MultiCast Counter whose value is assigned by the Dataflow Chip 202 ref. by page 5 para. [0084]-[0085], page 6 para. [0106]), a direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), and to de-allocate said storage element in response to a determination that said transmit count value is equal to a release count value (Fig. 5, the comparison of the MCC to the value of zero followed by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues ref. by page 5 para. [0084]-[0086]). Basso does not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data nor a processing element to determine a release count value of said storage element nor storage of count values within said storage element.

Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, the Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output ref. by col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Basso and Tezuka do not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data nor storage of count values within said storage element.

Gulick teaches a memory controller incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of providing control

signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Hooper teaches storage of count values within a storage element (transmit count stored in the primary packet descriptor ref. by page 3 para. [0025]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multicast data transmission method of Hooper to the dual port Packet Buffer Multicast Data Structure of Basso, Tezuka and Gulick for the purpose of using multiple transmit processors to transmit packets as suggested by Hooper (Abstract lines 1-6).

Claim 18, Basso teaches said second line card (Fig. 2, the Dataflow Chip 202 ref. by page 3 para. [0059]), further including a line interface module to receive data from a communications network (Fig. 2, the Dataflow chip 202 interface to the Ethernet MAC interface 203 ref. by page 3 para. [0059]), wherein said input module to store packet data within a storage element (FIG. 2, the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers ref. by page 3 para. [0059], page 4 para. [0060]), and to initialize a transmit count value of said storage element (MCC of Fig. 5, the MultiCast Counter whose value is assigned by the Dataflow Chip 202 ref. by page 5 para. [0084]-[0085], page 6 para. [0106]), comprises an input module to receive a packet including said packet data from said line interface module (Fig. 2, the Embedded Processor Complex 209 receiving packet data from the Ethernet MAC interface 203 for table lookup with the Dataflow chip 202 storing the packet in the Datastore Memory 205 ref. by page 3 para. [0059], page 4 para. [0060]-[0061]), and to

allocate said storage element for said packet including said packet data (Fig. 5, Buffers $505_1 - 505_5$ allocated to store packet data ref. by page 5 para. [0084]-[0085]).

Claim 19, Basso teaches said second line card (Fig. 2, the Dataflow Chip 202 ref. by page 3 para. [0059]), further including a memory coupled to said memory controller to store said storage element (Fig. 2, the Dataflow chip 202 which acts as a memory controller to transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]).

Claim 20, Basso teaches said second line card (Fig. 2, the Dataflow Chip 202 ref. by page 3 para. [0059]), further including a line card interconnect interface module having a plurality of output interfaces coupled to said line card interconnect (Fig. 2, the Dataflow Chip 202 interconnection with the Ethernet MAC interface 203 which carries a plurality of output ports including 1xOC-192c 4xOC-48c 16xOC-12c 1x10Gb Ethernet and 10x1Gb Ethernet ref. by page 3 para. [0059]).

Claim 21, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), comprises a direct memory access controller to transmit said packet data from said storage element to said line card interconnect interface module (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 through the interconnection between the Dataflow chip 202 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]).

Claim 22, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of output interfaces (Fig. 2, Fig. 5, the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports ref. by page 5 para. [0084]-[0086]).

Claim 23, Basso teaches said packet data including a packet header (Fig. 4, the Message ID and Message Parameters ref. by page 5 para. [0075]-[0083]), and a packet body (Fig. 4, the Data ref. by page 5 para. [0075]-[0083]), wherein said input module to store packet data within a storage element (Fig. 2, the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic ref. by page 3 para. [0059], page 4 para. [0060], [0069]), and to initialize a transmit count value of said storage element (MCC of Fig. 5, MultiCast Counter value stored by the Dataflow Chip based on the multicast action ref. by page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]), comprises an input module to store said packet body within a common storage element (Fig. 5, Buffers $505_1 - 505_5$ to store packet data ref. by page 5 para. [0084]-[0085]), comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, the unique data for the instance written to the Frame Alteration Control Block 503 for different header data

to different output ports ref. by page 6 para. [0090]), and to associate each of said plurality of unique storage elements with said common storage element (the linkage of the FACB 503 to the Buffers $505_1 - 505_5$ of Fig. 5) . Basso does not teach said processing element to determine a release count value of said storage.

Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, col. 16 lines 17-31, Fig. 23, the Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output ref. by col. 18 lines 60-67, col. 19 lines 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Claim 24, arguments analogous to those stated in the rejection of claim 17 are applicable.

Claim 25, arguments analogous to those stated in the rejection of claim 18 are applicable.

Claim 26, arguments analogous to those stated in the rejection of claim 19 are applicable.

Claim 27, arguments analogous to those stated in the rejection of claim 20 are applicable.

Claim 28, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), comprises a direct memory access controller to transmit said packet data from said storage element via said plurality of output interfaces (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 which has a plurality of output ports including 1xOC-192c 4xOC-48c 16xOC-12c 1x10Gb Ethernet and 10x1Gb Ethernet ref. by page 3 para. [0059], page 4 para. [0060], [0069]).

Claim 30, arguments analogous to those stated in the rejection of claim 23 are applicable.

Claim 41, Basso teaches a method comprising storing a plurality of packet data within a plurality of storage elements (Buffers $505_1 - 505_5$ of Fig. 5, Buffers $505_1 - 505_5$ to store a plurality of packet data ref. by page 5 para. [0084]-[0085]), maintaining a transmit count value of each one of said plurality of storage elements storing a plurality of packet data (MCC of Fig. 5, MultiCast Counter MCC for each packet to determine when all instances have been transmitted from the respective buffers and instances of plurality packets 505 ref. by page 5 para. [0084]-[0085]), comparing said transmit count value and a release count value for each one of said plurality of storage elements (Fig. 5, the comparison of the MCC to the value of zero for instance of the plurality of associated buffers 505 ref. by page 5 para. [0084]-[0085]), and de-allocating each one of said plurality of storage elements in response to comparing said transmit count value and a

release count value (Fig. 5, the discard of Frame Control Block 501 and its associated buffers $505_1 - 505_5$ by returning them to the free FCB and free buffer queues ref. by page 5 para. [0084]-[0086]). Basso does not teach determining a release count value of said storage element nor determining a release count value of each one of said plurality of storage elements nor maintaining a count value stored within each one of said plurality storage elements.

Tezuka teaches determining a release count value of of each one of said plurality of storage elements (Release Count Designation Unit 22-4 of Fig. 23, Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output wherein there are a plurality of discrete storage buffers for different buffer types ref. by col. 18 lines 60-67, col. 19 lines 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Basso and Tezuka do not teach maintaining a count value stored within each one of said plurality storage elements.

Hooper teaches maintaining a count value stored within each one of said plurality storage elements (transmit count stored in the primary packet descriptor ref. by page 3 para. [0025]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multicast data transmission method of Hooper to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of using multiple transmit processors to transmit packets as suggested by Hooper (Abstract lines 1-6).

Claim 42, Basso teaches further comprising transmitting each one of said plurality of packet data from said plurality of storage elements (Fig. 2, the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface wherein the Reference Frame Control Block has a Multicast Counter MCC for each plurality of packet data respectively ref. by page 4 para. [0069], Fig. 5, page 5 para. [0084]-[0086]).

Claim 43, Basso teaches wherein maintaining a transmit count value of said plurality of storage elements (MCC of Fig. 5, MultiCast Counter to determine when all instances have been transmitted for each FCB ref. by page 5 para. [0084]-[0085]), comprises initializing said transmit count value (Fig. 5, MultiCast Counter value stored by the Dataflow Chip based on the multicast action ref. by page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]). Basso, Tezuka and Hooper do not teach incrementing said transmit count value by one in response to transmitting said packet data.

Gulick teaches incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte

Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached ref. by col. 10 lines 29-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso, Tezuka and Hooper for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 44, Basso teaches wherein transmitting each one of said plurality of packet data from said plurality of storage elements (Fig. 2, the large Datastore Memory 205 as repository for multicast frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface ref. by page 4 para. [0069]), comprises transmitting each one of said plurality of packet data from one of said plurality of storage elements via a plurality of output interfaces (Fig. 2, Fig. 5, the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports ref. by page 5 para. [0084]-[0086]).

Claim 45, Basso teaches each one of said plurality of packet data including a packet header (Fig. 4, the Message ID and Message Parameters ref. by page 5 para. [0075]-[0083]), and a packet body (Fig. 4, the Data ref. by page 5 para. [0075]-[0083]), wherein storing said plurality of packet data within a storage element (Buffers 505_1 – 505_5 of Fig. 5, Buffers 505_1 – 505_5 to store packet data ref. by page 5 para. [0084]-[0085]), comprises storing said packet body within a common storage element (Fig. 5, Buffers

505_1 – 505_5 to store packet data ref. by page 5 para. [0084]-[0085]), storing a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports ref. by page 6 para. [0090]), and associating each of said plurality of unique storage elements with said common storage element (the linkage of the FACB 503 to the Buffers 505_1 – 505_5 of Fig. 5).

Claims 15, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basso, Tezuka, Gulick and Hooper as applied to claims 11, 13, 14, 24, 27, 28 above, and further in view of Chow et al. (Patent No. US 6269081 B1).

Claim 15, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by page 3 para. [0059], page 4 para. [0060], [0069]), via a plurality of line interfaces (Fig. 2, the Ethernet MAC interface 203 of various transmission protocol rates ref. by page 3 para. [0059]), comprises a direct memory access controller to transmit said packet data from said storage element via a line interface (Fig. 2, the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203 ref. by page 4 para. [0068]-[0069]), selected from the group consisting of an Ethernet interface (Fig. 2, the Ethernet MAC interface 203 ref. by page 3 para. [0059]), a Fast Ethernet Interface (Fig. 2, the Ethernet MAC interface 203 with 10Gb Ethernet

ref. by page 3 para. [0059]), a Gigabit Ethernet interface (Fig. 2, the Ethernet MAC interface 203 with 10x1Gb Ethernet ref. by page 3 para. [0059]), an OC-48/STM-16 interface (Fig. 2, the Packet Over Sonet interface 203 with 4xOC-48c ref. by page 3 para. [0059]), an OC-12/STM-14 interface (Fig. 2, the Packet Over Sonet interface 203 with 16xOC-12c ref. by page 3 para. [0059]). Basso, Tezuka, Gulick and Hooper do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, the OC-3 of 1.6 Gbps Access Shelf 3B ref. by col. 6 lines 7-45), an IF Video interface (Fig. 1, the FastBus Video of 800Mbps Access Shelf 3C ref. by col. 6 lines 7-45), a DS-1 interface (Fig. 1, DS-1 of 800Mbps Access Shelf 3D ref. by col. 6 lines 7-45), a DS-3 interface (Fig. 1, the DS-3 of 800Mbps Access Shelf 3C ref. by col. 6 lines 7-45), an E-1 interface (Fig. 1, the E-1 of 800Mbps Access Shelf 3D ref. by col. 6 lines 7-45), and an E-3 interface (Fig. 1, the E-3 of 800Mbps Access Shelf 3C ref. by col. 6 lines 7-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chow to the Multicast Data Structure of Basso, Tezuka, Gulick and Hooper for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Claim 29, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 ref. by

page 3 para. [0059], page 4 para. [0060], [0069]), via a plurality of output interfaces (Fig. 2, the Ethernet MAC interface 203 of various transmission protocol rates ref. by page 3 para. [0059]), comprises a direct memory access controller to transmit said packet data from said storage element via a line interface (Fig. 2, the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203 ref. by page 4 para. [0068]-[0069]), selected from the group consisting of an Ethernet interface (Fig. 2, the Ethernet MAC interface 203 ref. by page 3 para. [0059]), a Fast Ethernet Interface (Fig. 2, the Ethernet MAC interface 203 with 10Gb Ethernet ref. by page 3 para. [0059]), a Gigabit Ethernet interface (Fig. 2, the Ethernet MAC interface 203 with 10x1Gb Ethernet ref. by page 3 para. [0059]), an OC-48/STM-16 interface (Fig. 2, the Packet Over Sonet interface 203 with 4xOC-48c ref. by page 3 para. [0059]), an OC-12/STM-14 interface (Fig. 2, the Packet Over Sonet interface 203 with 16xOC-12c ref. by page 3 para. [0059]). Basso, Tezuka, Gulick and Hooper do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, the OC-3 of 1.6 Gbps Access Shelf 3B ref. by col. 6 lines 7-45), an IF Video interface (Fig. 1, the FastBus Video of 800Mbps Access Shelf 3C ref. by col. 6 lines 7-45), a DS-1 interface (Fig. 1, DS-1 of 800Mbps Access Shelf 3D ref. by col. 6 lines 7-45), a DS-3 interface (Fig. 1, the DS-3 of 800Mbps Access Shelf 3C ref. by col. 6 lines 7-45), an E-1 interface (Fig. 1, the E-1 of 800Mbps Access Shelf 3D ref. by col. 6 lines 7-45), and an E-3 interface (Fig. 1, the E-3 of 800Mbps Access Shelf 3C ref. by col. 6 lines 7-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chow to the Multicast Data Structure of Basso, Tezuka, Gulick and Hooper for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Allowable Subject Matter

Claims 1-2, 5, 7-8, 31-32, 35, 37-38 would be allowed upon resolution of the objections to independent claims 1 and 31 stated above.

Claim 46 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

The applicant's argument regarding the limitations of independent claim 41 has been fully considered.

Regarding independent claim 41, the amendment incorporating limitation of "transmit count value of each one of said plurality of storage elements stored within each one of said plurality of storage elements" is revealed by a new prior art search as disclosed by Hooper. As such a new round of rejections are presented for claim group 41-45.

The applicant's arguments traversing the art of Basso has been fully considered. The MCC is stored in a reference FCB, not in the buffers. Hooper however discloses a

counter stored in the packet descriptor which is part of the data buffers. It would have been obvious to incorporate the counter into the packet buffer as taught by Hooper. Regarding independent claims 11, 17, 24, the applicant's arguments presented has been fully considered. The examiner respectfully traverses the arguments. The limitation "initialized a transmit count value" is disclosed by Basso in terms of the MultiCast Counter value stored by the Dataflow Chip (page 5 para. [0084]-[0085], page 6 para. [0104]-[0106]) which is the initial value of the MCC. The amended limitation "stored within said storage element" is taught by the newly disclosed teachings of Hooper. The "processing element to determine a release count value" is taught by Tezuka by the Release Count Designation Unit 22-4 of Fig. 23. As such all limitations are taught by the references and based on the newly revealed Hooper reference, a revised round of rejections are presented.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L. Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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